

PROGRAMMABLE OSCILLATOR

Ceramic Surface Mount **EP25** Series 5.0V_{DC}



PART NUMBERING GUIDE

EP25 00 ET T TS L- 24.000M - TR	
FREQUENCY TOLERANCE / STABILITY 00=±100ppm Max (Standard), 45=±50ppm Maximum	AVAILABLE OPTIONS Blank=Bulk (Standard) TR=Tape and Reel (pg L1)
OPERATING TEMP. RANGE Blank=-20°C to 70°C (Standard) ET=-40°C to 85°C	FREQUENCY
DUTY CYCLE Blank=50 ±10% (Standard), T=50 ±5%	OUTPUT TYPE L=TTL, C=HCMOS
PIN 1 CONNECTION TS=Tri-State, PD=Power Down	

ELECTRICAL SPECIFICATIONS

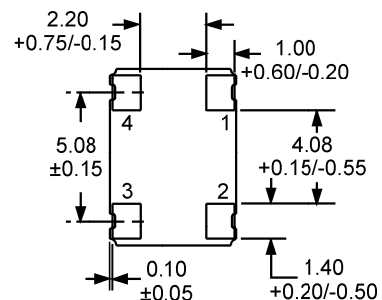
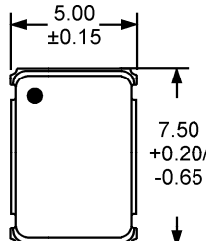
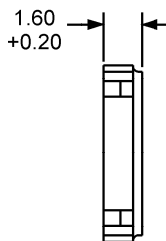
Marking Specifications See pg. G2, Group I

Frequency Range	1.000MHz to 125.000MHz	
Operating Temperature Range	-20°C to 70°C or -40°C to 85°C	
Storage Temperature Range	-55°C to 125°C	
Supply Voltage (V_{DD})	5.0V _{DC} ±10%	
Input Current	45mA Maximum (Unloaded)	
Disable Current (TS Option)	30mA Maximum (Pin 1=Ground)	
Standby Current (PD Option)	50uA Maximum (Pin 1=Ground)	
Frequency Tolerance / Stability	Inclusive of Operating Temp Range, Supply Voltage, and Load ±100ppm or ±50ppm Maximum	
Output Voltage Logic High (V_{OH})	w/TTL Load	2.4V _{DC} Minimum I _{OH} =-16mA
	w/HCMOS Load	V _{DD} - 0.4V _{DC} Minimum I _{OH} =-16mA
Output Voltage Logic Low (V_{OL})	w/TTL Load or w/HCMOS Load	0.4V _{DC} Maximum I _{OL} =+16mA
	w/TTL Load	4 nSeconds Max (0.8V _{DC} to 2.0 V _{DC})
Rise Time / Fall Time	w/HCMOS Load	4 nSec Max (20% to 80% of waveform)
	Duty Cycle	at 1.4V _{DC} w/TTL Load; at 50% of waveform w/HCMOS Load at 1.4V _{DC} w/TTL Load (≤ 27.000MHz only), or at 50% of waveform w/HCMOS Load (≤ 50.000MHz Only)
Load Drive Capability / Output Type-HCMOS	≤ 50.000MHz	50pF HCMOS Load Maximum
Load Drive Capability / Output Type-TTL	>50.000MHz	15pF HCMOS Load Maximum
Pin 1 Connection	TS	10TTL Load Maximum
	PD	5TTL Load Maximum
Pin 1 Input Voltage	V _{IH} : No Connection or ≥+2.0V _{DC}	Tri-State
	V _{IL} : (TS Option) ≤+0.8V _{DC}	Power Down
	V _{IL} : (PD Option) ≤+0.8V _{DC}	Enables Output
Aging (at 25°C)		Disable Output: High Impedance
Start Up Time		Disable Output: Logic Low
Absolute Clock Jitter	≤ 33.000MHz	±5ppm / year Maximum
	>33.000MHz	10 mSeconds Maximum
One Sigma Clock Period Jitter	≤33.000MHz	±250pSec Max, ±100pSec Typical
	>33.000MHz	±100pSec Max, ±50pSec Typical
		±50pSeconds Max
		±30pSeconds Max

MECHANICAL DIMENSIONS

Environmental / Mechanical Specifications See pg. H2, Group E

Pin 1: No Connect or Power Down	Pin 3: Output
Pin 2: Case Ground	Pin 4: Supply Voltage



Dimensions in mm

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Specifications subject to change without notice. • Contact factory for latest revision •1/99 • (OS48)